

# Notice of Allowability

Application No.

10/723,506

Examiner

Kaushikkumar Patel

Applicant(s)

CRADDOCK ET AL.

Art Unit

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to applicant's communication filed on 6/29/2006.
2. ☒ The allowed claim(s) is/are 1-3,5-12 and 14.
3. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
  - a) ☐ All b) ☐ Some\* c) ☐ None of the:
    1. ☐ Certified copies of the priority documents have been received.
    2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
    3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

\* Certified copies not received: \_\_\_\_\_.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.

**THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.**

4. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.
5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
  - (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
    - 1) ☐ hereto or 2) ☐ to Paper No./Mail Date \_\_\_\_\_.
  - (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date \_\_\_\_\_.

Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).
6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

## Attachment(s)

1. ☒ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3. ☐ Information Disclosure Statements (PTO/SB/08),  
Paper No./Mail Date \_\_\_\_\_
4. ☐ Examiner's Comment Regarding Requirement for Deposit  
of Biological Material
5. ☐ Notice of Informal Patent Application
6. ☐ Interview Summary (PTO-413),  
Paper No./Mail Date \_\_\_\_\_
7. ☒ Examiner's Amendment/Comment
8. ☒ Examiner's Statement of Reasons for Allowance
9. ☐ Other \_\_\_\_\_

## DETAILED ACTION

### EXAMINER'S AMENDMENT

1. An examiner's amendment to the record appears below. Should the changes and/or additions be unacceptable to applicant, an amendment may be filed as provided by 37 CFR 1.312. To ensure consideration of such an amendment, it MUST be submitted no later than the payment of the issue fee.

Authorization for this examiner's amendment was given in a telephone interview with Sean F. Sullivan (Reg. # 38,328) on September 1, 2006.

2. The application has been amended as follows:

**Claim 1** (currently amended): A method of managing memory mapped input output operations to an alternate address space comprising:

executing a first instruction directed to a first memory mapped input output alternate address space of a machine associated with a first adapter to allocate a resource associated with said first adapter to a selected process;

wherein said selected process issues at least one of a load and a store instruction executed in a problem state of said machine to a selected address location of a selected resource;

ensuring that said selected resource corresponds with said allocated resource;

determining that said selected resource corresponds with said process to which said resource is allocated; and

executing a second instruction for modifying a previously allocated resource, wherein said second instruction is a privileged instruction that is executed in [[a]] the supervisor state of [[a]] said machine.

**Claim 2** (currently amended): The method of Claim 1 further including a third instruction for freeing [[an]] the allocated resource of [[an]] said first adapter, wherein said third instruction is a privileged instruction that is executed in [[a]] the supervisor state of [[a]] said machine.

**Claim 3** (currently amended): The method of Claim 1 further including a fourth instruction for storing a previously allocated resource, wherein said fourth instruction is a privileged instruction that is executed in [[a]] the supervisor state of [[a]] said machine.

**Claim 5** (currently amended): A method of managing memory mapped input output operations to an alternate address space comprising:

executing a first instruction directed to a first memory mapped input output alternate address space of a machine associated with a first adapter to allocate a resource associated with said first adapter to a selected process;

wherein said selected process issues at least one of a load and a store instruction executed in a problem state of said machine to a selected address location of a selected resource;

ensuring that said selected resource corresponds with said allocated resource;

determining that said selected process corresponds with said process to which said resource is allocated; and

disabling a memory region in said first adapter such that said memory region may be enabled for another process, wherein said first instruction is a privileged instruction that is executed in a supervisor state of [[a]] said machine; and executing a second instruction for modifying a previously allocated resource, wherein said second instruction is a privileged instruction that is executed in the supervisor state of said machine.

**Claim 9** (currently amended): The method of Claim 1 wherein said first instruction is a privileged instruction that is executed in [[a]] the supervisor state of [[a]] said machine.

**Claim 10** (currently amended): The method of Claim 1 wherein said first adapter translates main-address-space virtual addresses on which said first adapter is operating into main-address-space real address within a given logical partition.

**Claim 11** (currently amended): The method of Claim 1 wherein said first adapter includes its own memory caching with respect to resource contexts.

**Claim 12** (currently amended): The method of Claim 11 wherein said first adapter caches its required memory contents from main memory of [[a]] said machine.

**Claim 14** (currently amended): A system of managing memory mapped input output operations to an alternate address space comprising:

a means for executing a first instruction directed to a first memory mapped input output alternate address space of a machine associated with a first adapter to allocate a resource associated with said first adapter to a selected process;

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wherein said selected process issues at least one of a load and a store instruction executed in a problem state of said machine to a selected address location of a selected resource;

a means for ensuring that said selected resource corresponds with said allocated resource; and

a means for determining that said selected resource corresponds with said process to which said resource is allocated; and

a means for executing a second instruction for modifying a previously allocated resource, wherein said second instruction is a privileged instruction that is executed in the supervisor state of said machine.

### ***Remarks***

3. During update search, a newly cited reference (US 2003/0046505 A1) suggested the motivation to disable allocated memory mapped region to an adapter in order to reallocate the allocated address space (reasons for previously indicated allowable claim 5), hence the claim 5 is further amended to include limitations from allowable claim 4.

### ***Allowable Subject Matter***

4. The following is an examiner's statement of reasons for allowance:

5. As per independent claims 1, 5 and 14, prior arts of record fails to teach an instruction for modifying previously allocated memory mapped resource of an adapter.

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Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

### ***Conclusion***

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Kaushikkumar Patel whose telephone number is 571-272-5536. The examiner can normally be reached on 8.00 am - 4.30 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mano Padmanabhan can be reached on 571-272-4210. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

  
MANO PADMANABHAN 9/5/06  
SUPERVISORY PATENT EXAMINER

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Kaushikkumar Patel

Examiner

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